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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,990	07/28/2003	Opher Kahn	42.P8917D	7335

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,990	KAHN ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on January 17, 2006.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 3-5 and 7-8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,662,278. Although the conflicting claims are not identical, they are not patentably distinct from each other

because the differences are obvious since claim 1 of U.S. Patent No. 6,662,278 fully encompasses claims 1, 3-5 and 7-8 in the instant application and the aforementioned claims of the instant application is an obvious anticipation of claim 1 in US Patent No. 6,662,278 based on the anticipation doctrine of *In re Goodman*.

4. Claims 9-12, 20-23, 24, and 26-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,662,278. Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences are obvious.

The major differences between the above conflicting claims is that claim 9 of the instant application calls for a chipset having a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it and a memory controller...etc and claims 20 and 24 call for a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it. Claim 1 of the aforementioned patent does not specify the device accessing the memory. However, a memory controller only accesses a memory in response to a received request. Additionally, the memory allocated to the memory controller effectively is allocated to the external device requesting the access the memory via the memory controller. Thus, although not indicated in the claim, it is evident that a source is requesting access to the memory via the memory controller and that the allocation of memory to the memory controller effectuates the same allocation upon the device(s) accessing the memory via the memory controller. It is well known in the art and conventional practice in the art for a processor to access memory via a memory controller and thus it would have been obvious to one

of ordinary skill in the art to do so for the desirable purpose of providing sufficient storage space to store data and programs for processing by the processor.

Claim Rejections - 35 USC § 112

5. Claims 9-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 9 and 24 include the feature, a processor having an original percentage of memory bandwidth allocated to it, however, the Examiner was not able to find any support in the specification for this claimed feature.

Claims 13-19 and 28-29 include the features, a graphics memory having an original percentage of graphics memory allocated to it; an individual I/O device having an original percentage of graphics memory bandwidth allocated to it, the graphics controller to increase the percentage....to decrease the percentage, etc.. However, the Examiner was not able to find any support in the specification for these claimed features.

Upon review of the sections noted by the Applicant as the relevant sections supporting newly added claims 2-29, the Examiner was not able to find anything substantiating the features mentioned above. Section [0040] of the specification only provides that the main memory receives request from a processor, graphics device or I/O device. The section further notes that the source of requests to access memory is not important to the present invention.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-12 and 20-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin (USPN: 5,953,685) in view of Woo (USPN: 6,021,076).

Regarding claims 1 and 5, Bogin discloses allocating an original percentage of bandwidth or number of accesses to memory by a memory controller (C 4, L 16-22; bandwidth of device prior to activation of the throttling regime) and decreasing the bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller (C 4, L 37-45, L 54-59). Bogin does not disclose increasing the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller. However, Woo teaches the concept of increasing the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to

the memory controller (C 9, L 60-67; C 10, L 1-10; C 6, L 1-15 – if the temperature [and thus the corresponding operating conditions [bandwidth] of the memory of the device at that instance] is below a threshold, thermal regulation is disabled which effectively increases the memory bandwidth). This feature allows the system to perform optimally when the temperature of the device is within a desired range. Hence it would have been obvious to one of ordinary skill in the art to use the teachings of Woo with the teachings of Bogin for the desirable purpose of optimization and to achieve maximum performance. Regarding claim 5, hardware devices such as memory controllers are controlled/operated by software stored in a machine-accessible medium.

Regarding claims 2 and 6, Bogin and Woo disclose setting a window of time to monitor the percentage of bandwidth or number of accesses to memory by the memory controller (Bogin - Figure 3B, Reference 300; C 5, L 11-19); and measuring the percentage of bandwidth used or number of accesses to memory by the memory controller during the window of time (Bogin -C 5, L 19-31).

Regarding claims 3 and 7, Bogin does not disclose applying a mask to increase the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller. However Bogin and Woo disclose increasing the percentage of memory bandwidth or the number of memory accesses allocated to the memory controller

when memory accesses by the memory controller are less than the percentage of memory bandwidth or the number of memory accesses allocated to the memory controller (Woo -C 9, L 60-67; C 10, L 1-10; C 6, L 1-15 – if the temperature [and thus the corresponding operating conditions [bandwidth] of the memory of the device at that instance] is below a threshold, thermal regulation is disabled which effectively increases the memory bandwidth). Since Bogin effectuates changing the bandwidth of the memory by applying a mask, it is evident that the mask would be applied to increase the bandwidth also.

Regarding claims 4 and 8, Bogin and Woo disclose applying a mask to decrease the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller (C 7, L 63-67; C 8, L 1-12).

Regarding claims 9, 20 and 24, Bogin discloses a chipset (Figure 2A) having a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it (Figure 2A, Reference 108; C 4, L 16-22; bandwidth of device prior to activation of the throttling regime); a memory controller to decrease the bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller (C 4, L 37-45, L 54-59). Bogin does not disclose the memory controller increasing the bandwidth or

number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller. However, Woo teaches the concept of increasing the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller (C 9, L 60-67; C 10, L 1-10; C 6, L 1-15 – if the temperature [and thus the corresponding operating conditions [bandwidth] of the memory of the device at that instance] is below a threshold, thermal regulation is disabled which effectively increases the memory bandwidth). This feature allows the system to perform optimally when the temperature of the device is within a desired range. Hence it would have been obvious to one of ordinary skill in the art to use the teachings of Woo with the teachings of Bogin for the desirable purpose of optimization and to achieve maximum performance.

Regarding claims 10 and 21, Bogin and Woo disclose a first register in the memory controller to set the percentage of memory bandwidth or the number of memory accesses allocated to the memory controller (Bogin - Figure 3B, Reference 310; C 5, L 46-59); a second register in the memory controller to set a window of time to monitor a percentage of memory bandwidth or the number of memory accesses used by the memory controller (Bogin - Figure 3B, Reference 300; C 5, L 11-19); and a counter in the memory controller to measure the percentage of memory

bandwidth used or the number of memory accesses by the memory controller during the window of time (Bogin - Figure 3B, Reference 303; C 5, L 19-31).

Claims 11, 22 and 26 are rejected for the same rationale applied to claims 3 and 7 above.

Claims 12, 23 and 27 are rejected for the same rationale applied to claims 4 and 8 above.

Claim 25 is rejected for the same rationale applied to claim 2 above.

Allowable Subject Matter

8. Claims 13-19 and 28-29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

KNM

March 31, 2006